IN THE SPECIFICATION:

Page 8, last paragraph on page continuing to top of page 9.

Next, the operation of the nonvolatile semiconductor memory device of the second embodiment will be explained with reference to Fig. ~~3~~ 2. The reading and writing operations are the same as the first embodiment, and their explanations are therefore omitted. Accordingly, only the operation of a test mode will next be explained. The test mode circuit 110 outputs an output signal and the nonvolatile semiconductor memory device is set to the test mode by applying 8 V to a specific terminal of the address input terminal 10. 8 V is applied to all the word lines 220 since the row decoder 140 selects all the word lines 220 by the output signal of the test mode circuit 110. Further, the bias voltage with respect to the select line 250 is removed by the regulator 120. The column decoder turns off all the column switches 240 to set all the bit lines 230 to a non-selecting state. Thus, electric field stress is applied to all the memory cells 210. Since one word line among the word lines 220 is connected to the monitor pad 50, the voltage of the word line 220 is given to the monitor pad 50.